CLAIMS

1. A device for data stream analysing, comprising processor means including a program memory making it possible to parse a data stream in a way that is controlled by an interchangeable program.

2. A device according to claim 1, also including a multiplexable data stream delay-line for receiving said data stream, and multiplexing means for connecting different parts of the data stream to said processor means

3. A device according to claim 2, where the multiplexing means include multiplexing control means for automatically keeping track of where specific data is located in the delayline, making it possible to write programs for controlling the device that can start executing at any time after the data have arrived to the device, and without the need for starting execution at a specific time relative to when a data stream was entering the device.

4. A device according to claim 2, where said delayline comprises a 23 shift deep, 1 byte wide shift register.

5. A device according to claim 2, where the multiplexing control means automatically keeps track of where specific data is located in the delayline by the use of position registers (named tagfield and lastfield) that changes according to certain rules when a packet is forwarded in the delay line

6. A device according to claim 4, where the value of the position registers are changed in the following way; when a packet arrives, the tagfield register starts to increment for every byte; when the packet has come to its end, i.e., the packets DV (data valid) signal becomes false again, the tagfield register stops counting and the lastfield register starts to increment.

7. A device according to claim 5, which automatically keeps track of where specific data is located in the delayline, by the use of said dedicated position registers together with the use of the formula

$$p = tagfield + lastfield - wanted\_tag$$

and "p" is the position of the wanted byte in the delayline; "tagfield" is the value of the tagfield register; "lastfield" is the value of the lastfield register and "wanted_tag" is the position of the wanted byte relative to the beginning of the

packet

8. A device according to claim 1, including registers for making logical and/or arithmetic operations on data-stream data, before an actual comparison of the data with other data is executed.

9. A device according to claim 1, including stack memory means which enables the writing of programs with subroutines for reducing the need of large program memories.

10. A device according to claim 1, which includes a base address register for the compare processor to make it possible to reuse code to recognise a given pattern even if it start at different positions in a data stream.

11. A device according to claim 1, where the program memory is of double ported type.